What is claimed is :

1. A power model for a semiconductor integrated circuit,

wherein said power model comprises a logic gate circuit part representing an operating part of said semiconductor integrated circuit and an equivalent internal capacitive part representing a non-operating part of said semiconductor integrated circuit.

2. The power model as claimed in claim 1, wherein said power model is independently provided for each of plural power systems which are independent from each other and included in said semiconductor integrated circuit.

3. The power model as claimed in claim 1, wherein internal circuit configurations of said semiconductor integrated circuit are divided into plural blocks on the basis of arrangement informations, and said power model is provided for each of said plural blocks.

4. The power model as claimed in claim 1, wherein internal circuit configurations of said semiconductor integrated circuit are divided into plural groups, each of said plural groups comprises a same timing group which includes logic gate circuits having individual signal transmission delay times fallen in a group-belonging predetermined time range which belongs to each of said plural groups, and said power model is provided for

each of said plural groups.

5. The power model as claimed in claim 1, wherein said power model further comprises a signal source connected to said logic gate circuit part for supplying a frequency-fixed signal to said logic gate circuit part, so that said logic gate circuit part represents operating state parts of said semiconductor integrated circuit in accordance with said frequency-fixed signal, and said equivalent internal capacitive part represents non-operating state parts of said semiconductor integrated circuit.

6. The power model as claimed in claim 5, wherein said equivalent internal capacitive part further represents operating-irrelevant fixed parts of said semiconductor integrated circuit.

7. The power model as claimed in claim 6, wherein said logic gate circuit part is connected between first and second powers, and said equivalent internal capacitive part is also connected between said first and second powers.

8. The power model as claimed in claim 7, wherein said logic gate circuit part further comprises a single pair of an inverter circuit and a load capacitive element, and said inverter circuit is connected between said first and second powers and said load capacitive element is also connected between said first and second powers, and said load capacitive element is

placed between said inverter circuit and said equivalent internal capacitive part.

9. The power model as claimed in claim 8, wherein said load capacitive element comprises a series connection of a first load capacitance and a second load capacitance between said first and second powers, and an intermediate point between said first and second load capacitances is connected to an output terminal of said inverter circuit.

10. The power model as claimed in claim 9, wherein said equivalent internal capacitive part further comprises at least an equivalent internal capacitive element connected between said first and second powers.

11. The power model as claimed in claim 10, wherein a plurality of said equivalent internal capacitive element is connected between said first and second powers, and said equivalent internal capacitive element comprises a series connection of a capacitance and a resistance between said first and second powers.

12. The power model as claimed in claim 11, wherein said inverter circuit comprises a series connection of a p-channel MOS field effect transistor and an n-channel MOS field effect transistor, and gate electrodes of said p-channel and n-channel MOS field effect transistors are connected to a clock signal source for applying a clock signal to said gate electrodes

of said p-channel and n-channel MOS field effect transistors.

13. The power model as claimed in claim 7, wherein said logic gate circuit part further comprises plural pairs of an inverter circuit and a load capacitive element, and said inverter circuit is connected between said first and second powers and said load capacitive element is also connected between said first and second powers, and in each pair, said load capacitive element is placed closer to said equivalent internal capacitive part than said inverter circuit.

14. The power model as claimed in claim 13, wherein said load capacitive element comprises a series connection of a first load capacitance and a second load capacitance between said first and second powers, and an intermediate point between said first and second load capacitances is connected to an output terminal of said inverter circuit.

15. The power model as claimed in claim 14, wherein said equivalent internal capacitive part further comprises at least an equivalent internal capacitive element connected between said first and second powers.

16. The power model as claimed in claim 15, wherein a plurality of said equivalent internal capacitive element is connected between said first and second powers, and said equivalent internal capacitive element comprises a series connection of a capacitance and a resistance between

said first and second powers.

17. The power model as claimed in claim 16, wherein said inverter circuit comprises a series connection of a p-channel MOS field effect transistor and an n-channel MOS field effect transistor, and gate electrodes of said p-channel and n-channel MOS field effect transistors are connected to a clock signal source for applying a clock signal to said gate electrodes of said p-channel and n-channel MOS field effect transistors.

18. The power model as claimed in claim 1, wherein said equivalent internal capacitive part is placed between said logic gate circuit part and a power system side.

19. The power model as claimed in claim 1, wherein said power model is deigned for simulation to a current distribution over a circuit board on which said semiconductor integrated circuit is mounted.

20. The power model as claimed in claim 19, wherein said power model is deigned for an electro-magnetic interference simulation to an electromagnetic field distribution over a circuit board on which said semiconductor integrated circuit is mounted.

21. A method of designing a power model for a semiconductor integrated circuit, and said power model comprising a logic gate circuit part

and an equivalent internal capacitive part,

wherein operating-related informations of all gate circuits constituting said semiconductor integrated circuit are utilized in first sequential processes to prepare said logic gate circuit part of said power model, and

wherein non-operating-related informations of said all gate circuits constituting said semiconductor integrated circuit are utilized in second sequential processes separated from said first sequential processes to prepare said equivalent internal capacitive part of said power model.

22. The method as claimed in claim 21, wherein, in said first sequential processes, informations about gate widths of operating-state p-channel transistors in said operating-state of said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor ;

informations about gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits are utilized to decide a gate width of a model n-channel transistor ;

informations about gate capacities of said operating-state p-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state p-channel transistors and a first power are utilized to decide a model first load capacity ; and

informations about gate capacities of said operating-state n-channel transistors in said operating-state of said constituting gate

circuits and about interconnection capacitances between said operating-state n-channel transistors and a second power are utilized to decide a model second load capacity,

whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed.

23. The method as claimed in claim 22, wherein a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second

load capacities is designed.

24. The method as claimed in claim 22, wherein a half of a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

25. The method as claimed in claim 22, wherein a product of the number of said operating-state gate circuits and an averaged value of gate widths of said operating-state p-channel transistors in said operating-state

of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said operating-state gate circuits and an averaged value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state p-channel transistors and a second averaged value of interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state n-channel transistors and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

26. The method as claimed in claim 22, wherein a half of a product of the number of said operating-state gate circuits and an averaged value of

gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a product of the number of said operating-state gate circuits and an averaged value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state p-channel transistors and a second averaged value of interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state n-channel transistors and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

27. The method as claimed in claim 21, wherein, in said first

sequential processes, informations about gate widths of all p-channel transistors of said constituting gate circuits and an information about operational rate of operating-state p-channel transistors in said operating-state are utilized to decide a gate width of a model p-channel transistor ;

informations about gate widths of all n-channel transistors of said constituting gate circuits and an information about operational rate of operating-state n-channel transistors in said operating-state are utilized to decide a gate width of a model n-channel transistor ;

informations about gate capacities of said all p-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all p-channel transistors and a first power and informations about said operational rate are utilized to decide a model first load capacity ; and

informations about gate capacities of said all n-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all n-channel transistors and a second power and informations about said operational rate are utilized to decide a model second load capacity,

whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed.

28. The method as claimed in claim 27, wherein a product of the

number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

29. The method as claimed in claim 27, wherein a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

30. The method as claimed in claim 27, wherein a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second

load capacities is designed.

31. The method as claimed in claim 27, wherein a half of a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of

p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

32. The method as claimed in claim 21, wherein, in said first sequential processes, informations about gate widths of all p-channel transistors of said constituting gate circuits and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor ;

informations about gate widths of all n-channel transistors of said constituting gate circuits and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a gate width of a model n-channel transistor ;

informations about gate capacities of said all p-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all p-channel transistors and a first power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model first load capacity ; and

informations about gate capacities of said all n-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all n-channel transistors and a second power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model second load capacity,

whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed.

33. The method as claimed in claim 32, wherein a product of the number of said all gate circuits, and a power current ratio of an averaged current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said all gate circuits, said power current ratio, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

34. The method as claimed in claim 32, wherein a half of a product of the number of said all gate circuits, and a power current ratio of an averaged current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a product of the number of said all gate circuits, said power current ratio, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

35. The method as claimed in claim 21, wherein, in said second sequential processes, informations about ON-resistances of non-operating-state transistors in said non-operating-state of said constituting gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity ; and

informations about gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

36. The method as claimed in claim 35, wherein a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating p-channel transistors in said non-operating state is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating n-channel transistors in said non-operating state is defined to be an ON-resistance of a second equivalent internal capacity ;

an arithmetic mean of a sum of gate capacities of said

non-operating p-channel transistors and a sum of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

an arithmetic mean of a sum of gate capacities of said non-operating n-channel transistors and a sum of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

37. The method as claimed in claim 35, wherein a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ;

and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

38. The method as claimed in claim 21, wherein, in said second sequential processes, informations about an averaged value of ON-resistances of all transistors included in said constituting gate circuits and the number of non-operating gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity ; and

informations about an averaged value of gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and the number of non-operating gate circuits as well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

39. The method as claimed in claim 38, wherein the number of

non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said semiconductor integrated circuit and a remainder by subtracting an average operational rate from 1 ;

a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at

least said equivalent internal capacity is designed.

40. The method as claimed in claim 38, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said semiconductor integrated circuit and a remainder by subtracting a maximum operational rate from 1 ;

a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of

interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

41. The method as claimed in claim 21, wherein informations about an averaged value of ON-resistances of all transistors included in said constituting gate circuits and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity ; and

informations about an averaged value of gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and informations about currents of basic gate circuits and said constituting gate circuits as well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

42. The method as claimed in claim 41, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of the total number of the constituting gate circuits included in the semiconductor integrated circuit and a power current ratio which is defined

to be a ratio of an averaged current value of all of basic gate circuits to an averaged current value of all of the constituting gate circuits ;

a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

43. The method as claimed in claim 21, wherein said equivalent internal capacitive part is placed between said logic gate circuit part and a power system side.

44. The method as claimed in claim 21, wherein said power model is deigned for simulation to a current distribution over a circuit board on which said semiconductor integrated circuit is mounted.

45. The method as claimed in claim 44, wherein said power model is deigned for an electro-magnetic interference simulation to an electromagnetic field distribution over a circuit board on which said semiconductor integrated circuit is mounted.

46. A storage medium for storing a computer program for designing a power model for a semiconductor integrated circuit, and said power model comprising a logic gate circuit part and an equivalent internal capacitive part,

wherein operating-related informations of all gate circuits constituting said semiconductor integrated circuit are utilized in first sequential processes to prepare said logic gate circuit part of said power model, and

wherein non-operating-related informations of said all gate circuits constituting said semiconductor integrated circuit are utilized in second sequential processes separated from said first sequential processes

to prepare said equivalent internal capacitive part of said power model.

47. The storage medium as claimed in claim 46, wherein, in said first sequential processes, informations about gate widths of operating-state p-channel transistors in said operating-state of said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor ;

informations about gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits are utilized to decide a gate width of a model n-channel transistor ;

informations about gate capacities of said operating-state p-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state p-channel transistors and a first power are utilized to decide a model first load capacity ; and

informations about gate capacities of said operating-state n-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state n-channel transistors and a second power are utilized to decide a model second load capacity,

whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed.

48. The storage medium as claimed in claim 27, wherein a sum of

gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

49. The storage medium as claimed in claim 47, wherein a half of a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is

defined to be a gate width of a model n-channel transistor ;

a half of a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

50. The storage medium as claimed in claim 47, wherein a product of the number of said operating-state gate circuits and an averaged value of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said operating-state gate circuits and an averaged value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said

operating-state p-channel transistors and a second averaged value of interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state n-channel transistors and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

51. The storage medium as claimed in claim 47, wherein a half of a product of the number of said operating-state gate circuits and an averaged value of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a product of the number of said operating-state gate circuits and an averaged value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said operating-state gate

circuits and a sum of both a first averaged value of gate capacitances of said operating-state p-channel transistors and a second averaged value of interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state n-channel transistors and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

52. The storage medium as claimed in claim 46, wherein, in said first sequential processes, informations about gate widths of all p-channel transistors of said constituting gate circuits and an information about operational rate of operating-state p-channel transistors in said operating-state are utilized to decide a gate width of a model p-channel transistor ;

informations about gate widths of all n-channel transistors of said constituting gate circuits and an information about operational rate of operating-state n-channel transistors in said operating-state are utilized to

decide a gate width of a model n-channel transistor ;

informations about gate capacities of said all p-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all p-channel transistors and a first power and informations about said operational rate are utilized to decide a model first load capacity ; and

informations about gate capacities of said all n-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all n-channel transistors and a second power and informations about said operational rate are utilized to decide a model second load capacity,

whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed.

53. The storage medium as claimed in claim 52, wherein a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

54. The storage medium as claimed in claim 52, wherein a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate

circuits is defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

55. The storage medium as claimed in claim 52, wherein a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an averaged value of gate widths

of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

56. The storage medium as claimed in claim 52, wherein a half of a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a product of the number of said all gate circuits, said

maximum operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

57. The storage medium as claimed in claim 46, wherein, in said first sequential processes, informations about gate widths of all p-channel transistors of said constituting gate circuits and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor ;

informations about gate widths of all n-channel transistors of said constituting gate circuits and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a gate width of a model n-channel transistor ;

informations about gate capacities of said all p-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all p-channel transistors and a first power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model first load capacity ; and

informations about gate capacities of said all n-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all n-channel transistors and a second power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model second load capacity,

whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed.

58. The storage medium as claimed in claim 57, wherein a product of the number of said all gate circuits, and a power current ratio of an averaged current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate

widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said all gate circuits, said power current ratio, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

59. The storage medium as claimed in claim 57, wherein a half of a product of the number of said all gate circuits, and a power current ratio of an averaged current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate

widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a product of the number of said all gate circuits, said power current ratio, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

60. The storage medium as claimed in claim 46, wherein, in said second sequential processes, informations about ON-resistances of non-operating-state transistors in said non-operating-state of said constituting gate circuits are utilized to decide an ON-resistance of an

equivalent internal capacity ; and

informations about gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

61. The storage medium as claimed in claim 60, wherein a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating p-channel transistors in said non-operating state is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating n-channel transistors in said non-operating state is defined to be an ON-resistance of a second equivalent internal capacity ;

an arithmetic mean of a sum of gate capacities of said non-operating p-channel transistors and a sum of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

an arithmetic mean of a sum of gate capacities of said non-operating n-channel transistors and a sum of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at

least said equivalent internal capacity is designed.

62. The storage medium as claimed in claim 60, wherein a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

63. The storage medium as claimed in claim 46, wherein, in said second sequential processes, informations about an averaged value of ON-resistances of all transistors included in said constituting gate circuits and the number of non-operating gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity ; and

informations about an averaged value of gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and the number of non-operating gate circuits as well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

64. The storage medium as claimed in claim 63, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said semiconductor integrated circuit and a remainder by subtracting an average operational rate from 1 ;

a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

65. The storage medium as claimed in claim 63, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said semiconductor integrated circuit and a remainder by subtracting a maximum operational rate from 1 ;

a double of a product of an averaged value of ON-resistances of

non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

66. The storage medium as claimed in claim 46, wherein informations about an averaged value of ON-resistances of all transistors included in said constituting gate circuits and informations about currents

of basic gate circuits and said constituting gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity ; and

informations about an averaged value of gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and informations about currents of basic gate circuits and said constituting gate circuits as well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

67. The storage medium as claimed in claim 66, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of the total number of the constituting gate circuits included in the semiconductor integrated circuit and a power current ratio which is defined to be a ratio of an averaged current value of all of basic gate circuits to an averaged current value of all of the constituting gate circuits ;

a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a

reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

68. The storage medium as claimed in claim 46, wherein said equivalent internal capacitive part is placed between said logic gate circuit part and a power system side.

69. The storage medium as claimed in claim 46, wherein said power model is deigned for simulation to a current distribution over a circuit board on which said semiconductor integrated circuit is mounted.

70. The storage medium as claimed in claim 69, wherein said power model is deigned for an electro-magnetic interference simulation to an electromagnetic field distribution over a circuit board on which said semiconductor integrated circuit is mounted.

71. A supporting system for designing a power model for a semiconductor integrated circuit, and said power model comprising a logic gate circuit part and an equivalent internal capacitive part, and said supporting system comprising :

a data base storing informations of internal circuit configurations ;

a storage medium for storing informations about circuit elements and interconnections between said circuit elements of said power model as well as for storing a computer program for designing said power model ;

a processor being connected to said data base and said storage medium for executing said computer program to prepare said power model ; and

an output device being connected to said processor for outputting said power model prepared by said processor,

wherein operating-related informations of all gate circuits constituting said semiconductor integrated circuit are utilized in first sequential processes to prepare said logic gate circuit part of said power model, and

wherein non-operating-related informations of said all gate

circuits constituting said semiconductor integrated circuit are utilized in second sequential processes separated from said first sequential processes to prepare said equivalent internal capacitive part of said power model.

72. The supporting system as claimed in claim 71, wherein, in said first sequential processes, informations about gate widths of operating-state p-channel transistors in said operating-state of said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor ;

informations about gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits are utilized to decide a gate width of a model n-channel transistor ;

informations about gate capacities of said operating-state p-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state p-channel transistors and a first power are utilized to decide a model first load capacity ; and

informations about gate capacities of said operating-state n-channel transistors in said operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state n-channel transistors and a second power are utilized to decide a model second load capacity,

whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed.

73. The supporting system as claimed in claim 52, wherein a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

74. The supporting system as claimed in claim 72, wherein a half of a sum of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a sum of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a sum of gate capacitances of said operating-state p-channel transistors and interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a sum of gate capacitances of said operating-state n-channel transistors and interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

75. The supporting system as claimed in claim 72, wherein a product of the number of said operating-state gate circuits and an averaged value of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said operating-state gate circuits and an averaged value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state p-channel transistors and a second averaged value of interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state n-channel transistors and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

76. The supporting system medium as claimed in claim 72, wherein a half of a product of the number of said operating-state gate circuits and an averaged value of gate widths of said operating-state p-channel transistors in said operating-state of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a product of the number of said operating-state gate circuits and an averaged value of gate widths of operating-state n-channel transistors in said operating-state of said constituting gate circuits is

defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state p-channel transistors and a second averaged value of interconnection capacitances between said operating-state p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said operating-state gate circuits and a sum of both a first averaged value of gate capacitances of said operating-state n-channel transistors and a second averaged value of interconnection capacitances between said operating-state n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

77. The supporting system as claimed in claim 71, wherein, in said first sequential processes, informations about gate widths of all p-channel transistors of said constituting gate circuits and an information about operational rate of operating-state p-channel transistors in said operating-state are utilized to decide a gate width of a model p-channel transistor ;

informations about gate widths of all n-channel transistors of said

constituting gate circuits and an information about operational rate of operating-state n-channel transistors in said operating-state are utilized to decide a gate width of a model n-channel transistor ;

informations about gate capacities of said all p-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all p-channel transistors and a first power and informations about said operational rate are utilized to decide a model first load capacity ; and

informations about gate capacities of said all n-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all n-channel transistors and a second power and informations about said operational rate are utilized to decide a model second load capacity,

whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed.

78. The supporting system as claimed in claim 77, wherein a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths

of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

79. The supporting system as claimed in claim 77, wherein a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a product of the number of said all gate circuits, an

average operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said all gate circuits, an average operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

80. The supporting system as claimed in claim 77, wherein a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

81. The supporting system as claimed in claim 77, wherein a half of a product of the number of said all gate circuits, a maximum operational rate of said gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined

to be a gate width of a model p-channel transistor ;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said all gate circuits, said maximum operational rate of said gate circuits, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

82. The supporting system as claimed in claim 71, wherein, in said first sequential processes, informations about gate widths of all p-channel transistors of said constituting gate circuits and informations about currents

of basic gate circuits and said constituting gate circuits are utilized to decide a gate width of a model p-channel transistor ;

informations about gate widths of all n-channel transistors of said constituting gate circuits and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a gate width of a model n-channel transistor ;

informations about gate capacities of said all p-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all p-channel transistors and a first power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model first load capacity ; and

informations about gate capacities of said all n-channel transistors of said constituting gate circuits and informations about interconnection capacitances between said all n-channel transistors and a second power and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide a model second load capacity,

whereby said logic gate circuit part comprising at least a pair of p-channel and n-channel transistors and at least a pair of first and second load capacities is designed.

83. The supporting system as claimed in claim 82, wherein a product of the number of said all gate circuits, and a power current ratio of an

averaged current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a product of the number of said all gate circuits, said power current ratio, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising a single pair of p-channel and n-channel transistors and a single pair of first and second load capacities is designed.

84. The supporting system as claimed in claim 82, wherein a half of a product of the number of said all gate circuits, and a power current ratio

of an averaged current value of said basic gate circuits to an averaged current value of said constituting gate circuits, and an averaged value of gate widths of said all p-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model p-channel transistor ;

a half of a product of the number of said all gate circuits, said power current ratio, and an averaged value of gate widths of all n-channel transistors in said all of said constituting gate circuits is defined to be a gate width of a model n-channel transistor ;

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all p-channel transistors and a second averaged value of interconnection capacitances between said all p-channel transistors and said first power is defined to be a model first load capacity ; and

a half of a product of the number of said all gate circuits, said power current ratio, and a sum of both a first averaged value of gate capacitances of said all n-channel transistors and a second averaged value of interconnection capacitances between said all n-channel transistors and said second power is defined to be a model second load capacity,

whereby said logic gate circuit part comprising two pairs of p-channel and n-channel transistors and two pairs of first and second load capacities is designed.

85. The supporting system as claimed in claim 71, wherein, in said second sequential processes, informations about ON-resistances of

non-operating-state transistors in said non-operating-state of said constituting gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity ; and

informations about gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits and about interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

86. The supporting system as claimed in claim 85, wherein a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating p-channel transistors in said non-operating state is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a reciprocal of a sum of reciprocals of ON-resistances of non-operating n-channel transistors in said non-operating state is defined to be an ON-resistance of a second equivalent internal capacity ;

an arithmetic mean of a sum of gate capacities of said non-operating p-channel transistors and a sum of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

an arithmetic mean of a sum of gate capacities of said non-operating n-channel transistors and a sum of interconnection capacities between said non-operating n-channel transistors and a second power is

defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

87. The supporting system as claimed in claim 85, wherein a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

88. The supporting system as claimed in claim 71, wherein, in said second sequential processes, informations about an averaged value of ON-resistances of all transistors included in said constituting gate circuits and the number of non-operating gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity ; and

informations about an averaged value of gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and the number of non-operating gate circuits as well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

89. The supporting system as claimed in claim 88, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said semiconductor integrated circuit and a remainder by subtracting an average operational rate from 1 ;

a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a

reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

90. The supporting system as claimed in claim 88, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of a total number of said constituting logic gate included in said semiconductor integrated circuit and a remainder by subtracting a

maximum operational rate from 1 ;

a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

91. The supporting system as claimed in claim 71, wherein

informations about an averaged value of ON-resistances of all transistors included in said constituting gate circuits and informations about currents of basic gate circuits and said constituting gate circuits are utilized to decide an ON-resistance of an equivalent internal capacity ; and

informations about an averaged value of gate capacities of said non-operating-state transistors in said non-operating-state of said constituting gate circuits, and informations about currents of basic gate circuits and said constituting gate circuits as well as informations about an averaged value of interconnection capacitances between said operating-state transistors and a power are utilized to decide said equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

92. The supporting system as claimed in claim 91, wherein the number of non-operating gate circuits in said non-operating state is defined to be a product of the total number of the constituting gate circuits included in the semiconductor integrated circuit and a power current ratio which is defined to be a ratio of an averaged current value of all of basic gate circuits to an averaged current value of all of the constituting gate circuits ;

a double of a product of an averaged value of ON-resistances of non-operating p-channel transistors in said non-operating state and a reciprocal of the number of non-operating gate circuits is defined to be an ON-resistance of a third equivalent internal capacity ;

a double of a product of an averaged value of ON-resistances of non-operating n-channel transistors in said non-operating state and a reciprocal of the number of said non-operating gate circuit is defined to be an ON-resistance of a second equivalent internal capacity ;

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating p-channel transistors and an averaged value of interconnection capacities between said non-operating p-channel transistors and a first power is defined to be said second equivalent internal capacity ; and

a product of said number of said non-operating gate circuit and an arithmetic mean of an averaged value of gate capacities of said non-operating n-channel transistors and an averaged value of interconnection capacities between said non-operating n-channel transistors and a second power is defined to be said third equivalent internal capacity,

whereby said equivalent internal capacitive part comprising at least said equivalent internal capacity is designed.

93. The supporting system as claimed in claim 71, wherein said equivalent internal capacitive part is placed between said logic gate circuit part and a power system side.

94. The supporting system as claimed in claim 71, wherein said power model is deigned for simulation to a current distribution over a

circuit board on which said semiconductor integrated circuit is mounted.

95. The supporting system as claimed in claim 94, wherein said power model is deigned for an electro-magnetic interference simulation to an electromagnetic field distribution over a circuit board on which said semiconductor integrated circuit is mounted.

96. The supporting system as claimed in claim 71, wherein said computer program further includes a first simulation program for analysis to circuits.

97. The supporting system as claimed in claim 96, wherein said first simulation program is to obtain a current distribution over a circuit board on which said semiconductor integrated circuit is mounted.

98. The supporting system as claimed in claim 97, wherein said computer program further more includes a second simulation program for analysis to electromagnetic field to obtain a distribution of electromagnetic field over said circuit board on which said semiconductor integrated circuit is mounted.

99. A simulator for simulating an electro-magnetic interference, said simulator comprising :

a circuit analyzing simulator being accessible to a first storage

medium for receiving a power model for a semiconductor integrated circuit, and also being connected to a second storage medium for receiving informations about a circuit board on which said semiconductor integrated circuit is mounted, so that said circuit analyzing simulator analyzes said power model to obtain a current distribution over a circuit board on which said semiconductor integrated circuit is mounted ;

an electromagnetic field analyzing simulator being accessible to said circuit analyzing simulator for receiving said current distribution, so that said electromagnetic field analyzing simulator analyzes an electromagnetic field distribution over said circuit board on which said semiconductor integrated circuit is mounted,

wherein said power model comprises a logic gate circuit part representing an operating part of said semiconductor integrated circuit and an equivalent internal capacitive part representing a non-operating part of said semiconductor integrated circuit.

100. The simulator as claimed in claim 99, wherein said power model is independently provided for each of plural power systems which are independent from each other and included in said semiconductor integrated circuit.

101. The simulator as claimed in claim 99, wherein internal circuit configurations of said semiconductor integrated circuit are divided into plural blocks on the basis of arrangement informations, and said power

model is provided for each of said plural blocks.

102. The simulator as claimed in claim 99, wherein internal circuit configurations of said semiconductor integrated circuit are divided into plural groups, each of said plural groups comprises a same timing group which includes logic gate circuits having individual signal transmission delay times fallen in a group-belonging predetermined time range which belongs to each of said plural groups, and said power model is provided for each of said plural groups.

103. The simulator as claimed in claim 99, wherein said power model further comprises a signal source connected to said logic gate circuit part for supplying a frequency-fixed signal to said logic gate circuit part, so that said logic gate circuit part represents operating state parts of said semiconductor integrated circuit in accordance with said frequency-fixed signal, and said equivalent internal capacitive part represents non-operating state parts of said semiconductor integrated circuit.

104. The simulator as claimed in claim 103, wherein said equivalent internal capacitive part further represents operating-irrelevant fixed parts of said semiconductor integrated circuit.

105. The simulator as claimed in claim 104, wherein said logic gate circuit part is connected between first and second powers, and said

equivalent internal capacitive part is also connected between said first and second powers.

106. The simulator as claimed in claim 105, wherein said logic gate circuit part further comprises a single pair of an inverter circuit and a load capacitive element, and said inverter circuit is connected between said first and second powers and said load capacitive element is also connected between said first and second powers, and said load capacitive element is placed between said inverter circuit and said equivalent internal capacitive part.

107. The simulator as claimed in claim 106, wherein said load capacitive element comprises a series connection of a first load capacitance and a second load capacitance between said first and second powers, and an intermediate point between said first and second load capacitances is connected to an output terminal of said inverter circuit.

108. The simulator as claimed in claim 107, wherein said equivalent internal capacitive part further comprises at least an equivalent internal capacitive element connected between said first and second powers.

109. The simulator as claimed in claim 108, wherein a plurality of said equivalent internal capacitive element is connected between said first and second powers, and said equivalent internal capacitive element

comprises a series connection of a capacitance and a resistance between said first and second powers.

110. The simulator as claimed in claim 109, wherein said inverter circuit comprises a series connection of a p-channel MOS field effect transistor and an n-channel MOS field effect transistor, and gate electrodes of said p-channel and n-channel MOS field effect transistors are connected to a clock signal source for applying a clock signal to said gate electrodes of said p-channel and n-channel MOS field effect transistors.

111. The simulator as claimed in claim 105, wherein said logic gate circuit part further comprises plural pairs of an inverter circuit and a load capacitive element, and said inverter circuit is connected between said first and second powers and said load capacitive element is also connected between said first and second powers, and in each pair, said load capacitive element is placed closer to said equivalent internal capacitive part than said inverter circuit.

112. The simulator as claimed in claim 111, wherein said load capacitive element comprises a series connection of a first load capacitance and a second load capacitance between said first and second powers, and an intermediate point between said first and second load capacitances is connected to an output terminal of said inverter circuit.

113. The simulator as claimed in claim 112, wherein said equivalent internal capacitive part further comprises at least an equivalent internal capacitive element connected between said first and second powers.

114. The simulator as claimed in claim 113, wherein a plurality of said equivalent internal capacitive element is connected between said first and second powers, and said equivalent internal capacitive element comprises a series connection of a capacitance and a resistance between said first and second powers.

115. The simulator as claimed in claim 114, wherein said inverter circuit comprises a series connection of a p-channel MOS field effect transistor and an n-channel MOS field effect transistor, and gate electrodes of said p-channel and n-channel MOS field effect transistors are connected to a clock signal source for applying a clock signal to said gate electrodes of said p-channel and n-channel MOS field effect transistors.

116. The simulator as claimed in claim 99, wherein said equivalent internal capacitive part is placed between said logic gate circuit part and a power system side.